REMARKS

Claims 62-69 are pending in this Application. Claims 34-36 and 70-73 have been withdrawn. Applicants reserve the right to pursue the original claims and other claims in this and in other applications.

The Application has been carefully reviewed in light of the Office Action mailed on April 20, 2005. Reconsideration of all outstanding rejections and objections in view of the following remarks is respectfully requested.

Claims 62, 66, and 70 have been amended. Support for these amendments can found in the specification in ¶¶ 19 -24. No new matter has been added.

Claims 62-69 stand rejected under 35 U.S.C. § 102 (e) as being unpatentable in view of Seyyedy (U.S. Pat. No. 6,754,124). ("Seyyedy1"). Reconsideration is respectfully requested.

Claim 62 recites, inter alia, "A method of reading a resistive memory device comprising a plurality of stacked layers of resistive memory cells, each layer comprising an array of memory cells arranged in rows and columns in an X-Y plane, said plurality of stacked layers forming a plurality of slices of resistive memory cells, each slice arranged in rows and columns in Y-Z planes and having a single associated access transistor, said method comprising: applying a voltage to a read/write line associated with a selected memory cell from one of said plurality of slices of resistive memory cells; activating an access transistor associated with said selected memory cell; coupling selected memory cell through said selected memory cell to a sense amplifier; and sensing a logic state of said selected memory cell."

Seyyedy 1 discloses MRAM array where a single access transistor is used to operate the reading of a column segment. The invention of Seyyedy1 is different from the claimed invention (of Seyyedy and Nejad ("Nejad")), in that the claimed invention discloses "a plurality of ...memory slices, each slice ...having a single associated access

transistor." As such, the claimed invention is directed towards "memory slices." Furthermore, the claimed invention has a "single access transistor" per slice, which is different from the Seyyedy1's invention which discloses at least two "single access transistor[s]" per Y-Z plane. As such, Seyyedy1 fails to disclose the claimed invention. Therefore, the rejection of claim 62 should be withdrawn.

Claims 63-65 depend, directly or indirectly, from claim 62 and therefore these claims are allowable for at least the reasons noted above.

Claim 66 has a similar limitation as claim 62, "a plurality of memory slices, each....having a single associated access transistor," and claims 67-69 depend, directly or indirectly, from claim 66 and therefore these claims are allowable for at least the reasons noted above.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to pass this application to issue.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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